REMARKS

By this amendment, claim 1 has been amended, and claims 21 and 22 have been added. Thus, claims 1-4, 6, and 10-22 are now active in the application. Reexamination and reconsideration of the application are respectfully requested.

Initially, in item 8 on page 4 of the Office Action, the Examiner kindly indicated that claims 11-20 are allowed over the prior art of record. In the "Reasons for Allowance" in item 9 on page 4 of the Office Action, the Examiner indicated that "the prior art does not disclose nor fairly suggest a semiconductor device assembling method as provided in independent claim 11. The first surface to which the semiconductor element is formed has been polished while the second surface is finished in order to remove a damaged layer which makes a very thin semiconductor element."

On pages 2-4 of the Office Action, claims 1-4 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by Shiotsuka et al. (U.S. 6,174,075); and claims 6 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Shiotsuka et al. in view of Nakamura et al. (U.S. 6,300,576). These rejections are respectfully traversed, and in any event, are clearly inapplicable to the claims as now amended, for the following reasons.

With exemplary reference to the present drawing figures and, in particular, Figs. 1A and 1B, claim 1 sets forth a semiconductor device 1 comprising: a semiconductor element 2 that has a first surface (top surface in Fig. 1B) on which an external connection terminal 2a is formed and a second surface (bottom surface in Fig. 1B) opposite the first surface, and a thickness of 10μm or more and 150μm or less; a plate 4 that faces the second surface (bottom surface of the semiconductor element 2); and a resin binder 5 that adheres the second surface (bottom surface of the semiconductor of the element 2) and the plate 4, wherein the plate 4 has a rigidity higher than that of the semiconductor element 2; wherein the second surface (bottom surface) of the semiconductor element 2 comprises a surface-finished surface such that the second surface (bottom surface) of the semiconductor element 2 is free from having a damaged layer thereon (as described, for example, at page 6, line 23 - page 7, line 8 of the substitute specification); wherein an outer shape of the plate 4 is larger than that of the semiconductor element 2; and wherein the resin binder 5 covers a peripheral side face 2b (at 5a) of the semiconductor element 2, and

furthermore at a portion that is interposed between the second surface (bottom surface of the semiconductor element 2) and the plate 4 the resin binder 5 allows the semiconductor element 2 to deform in a thickness direction thereof.

Thus, claim 1 has been amended to include the limitation corresponding to the limitation referenced by the Examiner in connection with the allowability of allowable claim 11 (i.e., that the second surface of the semiconductor element 2 comprises a surface-finished surface such that the second surface of the semiconductor element 2 is free from having a damaged layer thereon). Also, claim 1 has been amended to clarify that the side face 2b is a peripheral side face of the semiconductor element 2. It is submitted that claim 1 clearly distinguishes over the Shiotsuka et al. patent which provides no teaching or suggestion that the semiconductor element thereof has a second surface which constitutes a surface-finished surface such that the second surface of the semiconductor element is free from having a damaged layer thereon, as required by claim 1.

Furthermore, it is submitted that there is no disclosure or suggestion in Shiotsuka et al. of a semiconductor element having a thickness of 10μm or more and 150μm or less. In this regard, if the Examiner is referring to the element 400 (Fig. 4) of Shiotsuka et al. as constituting the claimed semiconductor element, it is submitted that the Shiotsuka et al. patent does not disclose a particular thickness for the semiconductor element 400. At column 22, line 54 - column 23, line 8, the thicknesses of the various layers 402 - 404 of the semiconductor element 400 are mentioned, but a thickness of the fourth layer 401 of the semiconductor element 400 is not specified. The combined thicknesses of the elements 402 - 404 as mentioned in the above passage of the Shiotsuka et al. patent constitute an overall thickness of 15,950 Angstroms (which equals 1.595μm). If the Examiner is referring to the element 403 of the Shiotsuka et al. patent as the claimed semiconductor element, the element 403 is indicated as having a thickness of 5,250 Angstroms (0.525μm). Neither of these disclosed thicknesses are within or near the claimed thickness range.

Also, the Examiner has referred to the element 401 (Fig. 4) of Shiotsuka et al. as the claimed "plate" having a rigidity higher than that of the semiconductor element. However, the substrate (plate) 401 is a constituent element of the semiconductor element 400 and, accordingly, cannot be said to face the second surface of the semiconductor element.

In item 2 on page 2 of the Office Action, the Examiner indicated that Shiotsuka et al. discloses that "the resin binder covers a side face of the semiconductor element, and furthermore at a portion that is interposed between the second surface and the plate the resin binder allows the semiconductor element to deform in a thickness direction thereof (column 5, lines 57-67 thru column 6, lines 1-22)." However, this cited section of the Shiotsuka et al. patent provides no disclosure regarding a resin binder covering a side face of a semiconductor element, as asserted by the Examiner. In item 3 spanning pages 2 and 3 of the Office Action, the Examiner indicated that "regarding claim 2, Shiotsuka et al. discloses wherein the resin binder covers at least an edge that is formed of defined by [sic] a side face and the second surface of the semiconductor element about the outer periphery of the semiconductor element (column 14, lines 53-67)." However, contrary to this assertion, column 14, lines 53-67 of the Shiotsuka et al. patent does not disclose or suggest the resin binder that covers a peripheral side face of a semiconductor element, as well as a second surface, and wherein the resin binder adheres the second surface to the plate.

Thus, for at least the above reasons, it is believed apparent that the Shiotsuka et al. patent does not disclose or suggest the feature recited in claim 1 and, accordingly, that Shiotsuka et al. cannot be said to anticipate claim 1. It is noted that the Examiner has generally asserted that the various features of claim 1 (as presented in the Amendment filed December 28, 2006) are present in the Shiotsuka et al. patent, and has made general references to Fig. 4; column 14, lines 53-67; and column 5, lines 57-67 thru column 6, lines 1-22 of the Shiotsuka et al. patent. However, these references to the Shiotsuka et al. patent do not indicate where the features recited in claim 1 are located. Therefore, it is respectfully requested that, if the Examiner persists in this rejection, the Examiner provide specific references to locations in the Shiotsuka et al. patent to indicate locations of the patent where the specifically-recited features of claim 1 are disclosed.

The Examiner cited the Nakamura et al. patent for disclosing "wherein the external connection terminal is provided with a bump (column 1, lines 34-51)." However, the Nakamura et al. patent clearly does not provide any teaching or suggestion that would have obviated the above-discussed shortcomings of the present invention of claim 1.

Thus, for the above reasons, it is believed apparent that claim 1 is not anticipated by the Shiotsuka et al. patent. Furthermore, there is no teaching or suggestion in the Shiotsuka et al.

patent or in any other references of record which would have caused a person of ordinary skill in the art to find it obvious to modify Shiotsuka et al. or to make any combination of the references of record in such a manner as to result in or otherwise render obvious the present invention of claim 1. Therefore, it is respectfully submitted that claim 1, as well as claims 2-4, 6, 9, 10, 21 and 22 which depend therefrom, are clearly allowable over the prior art of record.

The Examiner's attention is next directed to the dependent claims which set forth additional features of the present invention and further define the invention over the prior art. For example, claim 21 specifies that a surface of the peripheral side face 2b of the semiconductor element 2 includes a micro crack, and the resin binder 5, 5a covering the peripheral side face of the semiconductor element 2 reinforces the peripheral side face 2b having the micro crack (see, for example, page 8, lines 14-25 of the substitute specification). Claim 22 specifies that, as illustrated in Fig. 1B, the first surface (top surface) of the semiconductor element 2 is exposed from the resin binder 5.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is earnestly solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, it is respectfully requested that the Examiner contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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